CMOS A/D Converter Interfaces Easily with Many Microprocessors

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With a span accommodation down to 180 mV, this 8-bit unit can also replace a 12-bit analog-to-digital device in some applications.

To help meet the rising demand for easier interfacing between analog-to-digital converters and microprocessors, the complementary MOS, 8-bit ADC0801-05 has been designed to accommodate almost all of today's popular microprocessors. It requires only a single 5V supply and is low power to boot.

Housed in a 20-pin dual-in-line package, the successive approximation device includes a Schmitt trigger circuit that allows it to be driven from a system clock, as well as an external RC network. At a clock frequency of 640 kHz, conversion time is 100 µs. What's more, its guaranteed linearity error of ±¼ least significant bit (typically ±1/16 LSB) can encode an analog signal span as small as 180 mV — a performance that allows it to replace 9, 10, and even 12-bit converters in many applications.

Constantly decreasing converter prices raise the comparative cost of the interface electronics and increase the demand for simplicity of interfacing. The growing emphasis on simpler systems for higher levels of reliability has also pushed this demand, as has a trend toward lower levels of power dissipation. And with the success of the 5V power supply standard of logic circuits, linear circuits have been pressed for 5V operation. Supporting the ADC0801-05 A/D converter are such special operational amplifiers as the LM358 dual and the LM324 and LM3900 quad op amps that run off 5V supplies; also useful are voltage comparators such as the LM393 dual and LM339 quad devices. Perhaps the most versatile of such 5V linear devices is the LM392, comprising an op amp and a comparator.

MORE COMPLICATIONS

Complicating the interfacing are the ever higher levels of resolution in monolithic converters, with 8 and 10-bit types readily available and 12-bit devices ready to emerge soon. Yet, despite their greater resolution, 10 and 12-bit monolithic A/D converters are not only more expensive than 8-bit designs, but also require more careful attention to system noise problems and management of grounding.

For simple interfacing, an A/D converter must operate directly with the signals available on a microprocessor control bus. The converter is generally given an address that can be mapped into memory or input/output space, depending on the type of microprocessor employed. On 6800 microprocessors and their derivatives, no special input/output addressing or strobes are available, so the converter must appear as a memory location to these processors. Z80® microprocessors, on the other hand, not only provide special I/O interfacing, but also automatically insert a wait state during I/O selection to increase the width of the read and write strobe signals. This eases interface requirements considerably, since slower I/O devices can operate with much faster microprocessor units. The automatic wait state for I/O devices will loom larger in importance as the next generation of higher speed microprocessors evolves.

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COMPATIBILITY CRITERIA DIFFER

Microprocessor compatibility has a wide range of meanings — at least according to the various converter data sheets. True compatibility, however, involves meeting electrical specifications like proper logic voltage levels with adequate loading capability. For example, true TTL compatibility means the ability to maintain a 0.4V low potential (or less) at the A/D converter logic outputs while sinking 1.6 mA of current. And the high state must be maintained at a minimum of 2.4V while supplying at least 360 µA.

Furthermore, all interface protocols must be met. This not only means operating with the proper signals, but also meeting all necessary timing requirements, so the converter must have valid data on the microprocessor bus within the access time of the memory system with which it happens to be working.

The protocols for interfacing are not at all standardized. Some A/D converters make use of the standard chip select signal ($\overline{CS}$) to start a conversion. But decoding voltage glitches can cause an A/D converter to begin conversion when it is not desirable. Both the standard $\overline{CS}$ signal and a write strobe signal ($\overline{WR}$) must therefore be used, so that the former signal qualifies the latter and prevents unwanted conversions due to address decoding glitches. Care must also be taken when using some A/D converters that are designed to act as bus controllers; problems can arise when the central processor is not in control of the bus.

DIFFERENT STANDARDS

The 8080 and 6800 microprocessors (and their derivatives) use different control bus standards. Microprocessors based on the 8080, for example, make use of read and write strobe signals to specify the operation (read or write) requested. Working with these microprocessors, A/D converters start the conversion cycle upon the microprocessor's issuance of a chip select signal (decoded from the address bus) and a write strobe signal. At the end of conversion (EOC), the converter issues an EOC signal. When dealing with older A/D converters where the EOC signal is typically low during the conversion process and high at the end of it, microprocessors have difficulty because the EOC signal is not available on the data bus. Furthermore, the EOC signal does not reset when the converter is serviced by the central processing unit (that is, when data has been read).

Complications can also occur when microprocessors interface with older A/D devices during read operations. For proper interfacing, such converters must have valid data on the bus within the memory access time.

Interfacing requirements differ for 6800-type microprocessors, like the 6502 and 68000, which use read/write (R/$\overline{W}$) control lines instead of read and write strobe signals and obtain timing information from the system clock signal. In addition, they include a valid memory address signal to qualify the address that is placed on the bus. Such features make interfacing for these microprocessors different from that for earlier 8080 types.

For an A/D converter to be most useful in a microprocessor-based system, it must have such desirable analog features as differential inputs, and it should adjust to accommodate various analog input signal ranges. The ADC0801-05 offers differential analog inputs, but it is the converter's span accommodation that allows many unusual and useful analog applications.

The availability of differential analog voltage inputs eliminates the problem of poor analog grounds, since both inputs can be connected directly across the analog signal source.

The negative (normally grounded) analog input lead can be referenced to any desired DC offset voltage to accommodate an input signal range that does not swing down to ground. A DC offset can thus be used at this input to cause a digital output of all 0s at any desired input voltage.

FLEXIBLE SPAN

Finally, the ability to accommodate an arbitrary span or input dynamic voltage range is desirable in an A/D converter. This can easily be achieved in the ADC0801-05 by selecting the magnitude of the converter's reference input.

An example might be to permit an analog input voltage range of 0.5V to 3.5V. This is accomplished by tying the converter's negative input lead to a 0.5 V_{DC} offset voltage and supplying a reference voltage that is equal to half the 3V span. This application provides the 00 output code for V_{IN} = 0.5 V_{DC} and the FF output code for V_{IN} = 3.5 V_{DC}.

In many applications (such as weighing cans on a production line), 14, or even 16-bit converters are often called upon for the needed high levels of resolution. For those reduced-span applications, an 8-bit A/D converter can be used instead — at considerable savings.

A SAMPLED-DATA INPUT

The ADC0801-05 makes use of a sampled-data comparator. Sampled-data circuits cancel the offset voltage, provide essentially temperature-independent performance, and cancel low frequency MOS 1/f noise. They do, however, provide some differences in application, since there is an input stray capacitance to ground, as shown in *Figure 1*.

When switch S1 is closed, stray input capacitance, C_{IN}, is charged to the input analog potential, V_{ANALOG}. Note that with a stray capacitance of approximately 12 pF and a 5 kΩ MOS switch resistance, the time constant, τ, is only 60 ns. Thus, C_{IN} becomes charged to the necessary accuracy level (within ±¼ LSB) in 6.9τ, or about 0.4 µs. Since the input switches are operating at one eighth the input clock frequency of 640 kHz, there is ample time for C_{IN} to settle, as comparisons are made only at the end of the clock period. Note that the switch at the (−) analog input discharges the stray capacitance; this event causes input displacement currents to flow.

Input bypass capacitors, when placed directly at the analog inputs, cause full-scale errors, since they average the current which will flow through the source resistance of the analog input signal generator. Input capacitors are not required; but if they are used, a full-scale adjustment will eliminate any system errors.

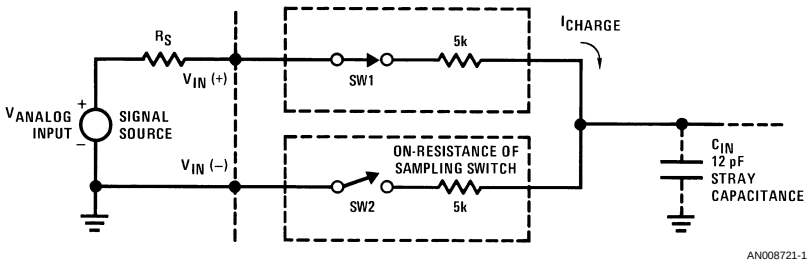

FIGURE 1. Equivalent. Because it has a sampled-data comparator input, the 8-bit ADC0801-05 monolithic analog-to-digital converter looks capacitive to an input signal source. The sampling switches operate at one eighth the rate of the clock frequency.

The ADC0801-05 monolithic 8-bit CMOS A/D converter can be operated with a wide range of $V_{REF}/2$ voltages that facilitates its use in many different circuit applications. Inexpensive ratiometric transducers, such as potentiometers, can be tied across the converter's 5V supply voltage with the wiper fed directly to the converter's V_{IN}+ input pin. The $V_{REF}/2$ pin, which will now bias at 2.5V, can be tied to a second potentiometer that is also hooked across the supply voltage to provide a full-scale adjustment.

When the $V_{REF}/2$ is grounded, the converter then functions as a comparator, yielding a digital output of all 1s when V_{IN}+ is greater than V_{IN}−, and of all 0s when V_{IN}+ is less than V_{IN}−. The $V_{REF}/2$ feature is also useful for low level analog voltage systems where an operational amplifier is normally used to boost the input signal prior to digitization. In a circuit with an analog input voltage of 250 mV maximum, for example, the signal can be fed directly to the A/D device, saving the cost of the amplifier. The $V_{REF}/2$ pin would thus be biased at 125 mV.

CAREFUL GROUNDING

A minor drawback is that this extra analog resolution leaves the circuit more susceptible to noise, and the $V_{REF}/2$ voltage requires a low initial tolerance and must be stable over temperature changes. Grounding problems become more critical and careful grounding is a must.

The ADC0801-05 can also be used as a logarithmic converter to extend the input voltage dynamic range to cover three decades. Three input logging circuits (*Figure 2*) are provided by the NPN transistors in the feedback loops of operational amplifiers. With these at the same temperature (all

three on a common chip), there are no thermal problems with this circuit. To keep costs at their lowest, the three transistors in the LM389 audio amplifier IC can be used.

The fourth operational amplifier in *Figure 2* is used to supply the proper $V_{REF}/2$ voltage to the A/D converter. Its DC output voltage is half that of the logarithmically compressed analog input voltage span.

OFFSET ADJUSTING

Yet another application for the ADC0801-05 is in automatically adjusting the offset voltage of an op amp under microprocessor control. This is useful in transducer bridge networks where a pair of amplifiers is normally used to amplify the differential signal. Such an output signal can be fed directly to the A/D converter's inputs without requiring a more costly instrumentation amplifier. The bridge network's arms will thus be biased at approximately $V_{CC}/2$.

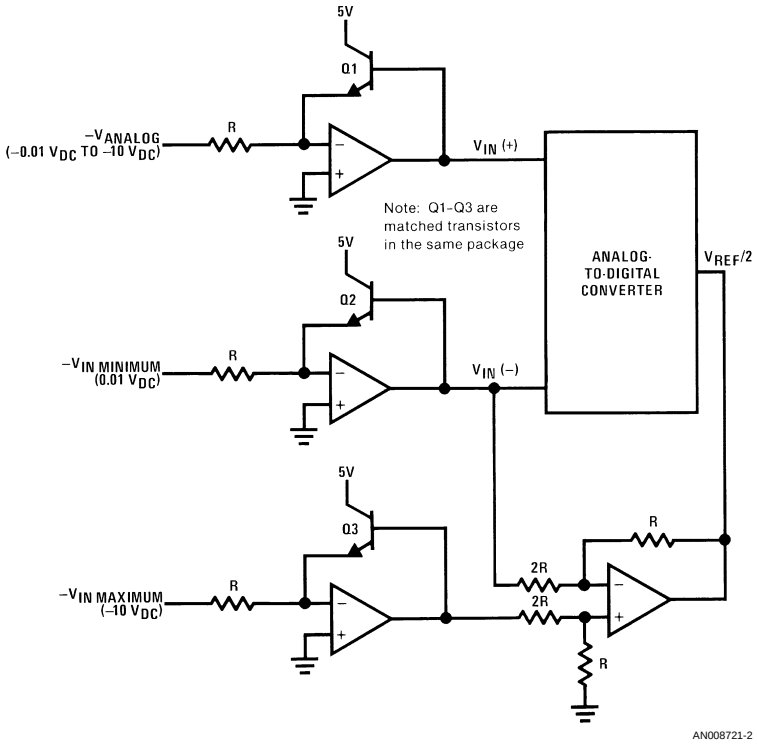

FIGURE 2. Logarithmic. The ADC0801-05 monolithic A/D converter's $V_{REF}/2$ pin allows its use as a three-decade logarithmic circuit. The three NPN transistors in the feedback loops of the operational amplifiers give better accuracy with changing temperature than the diodes normally used.

Figure 3 shows such a circuit, where the microprocessor takes the digital output of the A/D device and automatically adjusts the output voltage of operational amplifier 2. This amplifier is used to isolate the bridge network from the offset adjustment circuit. The INS8255 programmable peripheral interface controls the offset voltage adjustment and analog switches 1 and 2. The CMOS buffer provides ideal analog level swings of either 0V or 5V to the binary resistor network. The binary resistor network extracts and injects a current from and into op amp 3, causing a small voltage drop across R_S. This corrects for offset voltage that is introduced anywhere in the system.

AUTO ADJUSTMENT

Electrically actuated switches 1 and 2 allow the automatic adjustment of the offset voltage. It should be noted that op amp 1 is referenced to one side of the bridge network in order to cancel any common-mode offset voltage effects.

The A/D converter acts as a high gain comparator because a 0V $V_{REF}/2$ is provided by the voltage follower (amplifier 4) and switch 1 circuits. This allows the microprocessor to perform a successive approximation routine to null the offset

voltage of the system. Resolution is thus considerably better than the normal + 1LSB obtainable with a conventional A/D converter.

The ADC0801-05 combines linear and digital features in an A/D converter that is flexible and easy to tie to microprocessor-based systems. The benefits of a sampled-data comparator and an unusual ladder now make an A/D converter actually easier to fabricate than a digital-to-analog converter.

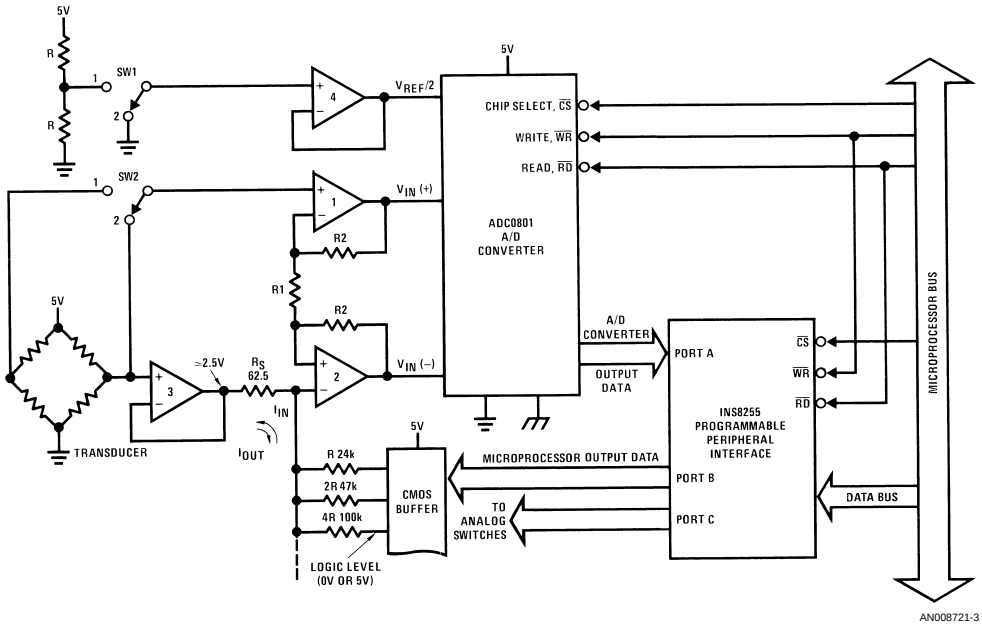

FIGURE 3. Automatic. Adjusting the offset voltage of a differential amplifier pair in a transcript bridge network can be done automatically. A microprocessor provides this adjustment through a programmable peripheral interface and a buffer integrated circuit.

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